Conclusions:

i) The output of circuits (Q and $\bar{Q}$) will always be complementary. i.e if $Q = 0$ then $\bar{Q} = 1$.

ii) The circuit has two stable states. One stable state corresponds to $Q = 1$, $\bar{Q} = 0$. and it is called set state. On the other hand, another stable state corresponds to $Q = 0$; $\bar{Q} = 1$ called reset state.

iii) If the circuit is on the reset state ($Q = 0$, $\bar{Q} = 1$) then it continues to be on the reset state. and vice versa.

iv) It can store 1 bit of digital information. Therefore it is called as 1 bit memory cell.

Latch: The cross-coupled inverters is known as latch because it is capable of locking or latching the information. The drawback of this circuit is that we can't enter the desired digital data into it.

This drawback is overcome by modifying the circuit as shown below which enters the desired digital data into the circuit.

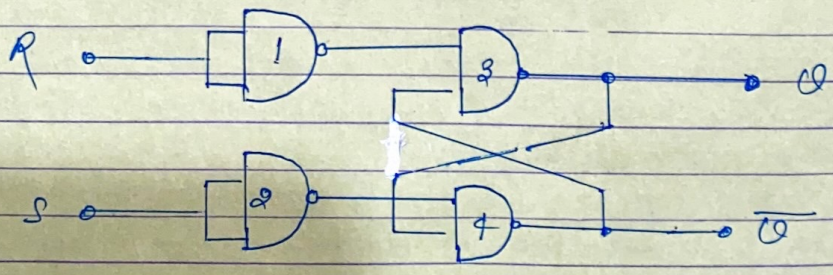


Fig: Modified memory cell.

Case-I $S=0, R=0$.

Let $Q=0$, and $\bar{Q}=1$. Therefore, both the inputs to gate-2 are 1 and the input to gate-1 are (01). So, o/p of gate-2 is $Q=0$ and $\bar{Q}=1$.
Then with $S=R=0$ there is no change in the state of outputs.

Case-II. $S=1, R=0$.

In this case one of the inputs to gate-2 will be 0. This forces Q output to 1. Therefore, both the I/p to gate-1 becomes 1. This forces $\bar{Q}$ to 0.
i.e $Q=1$ and $\bar{Q}=0$. This is called set.

Case-III : $S=0, R=1$

If $S=0$, $R=1$, then one of the input to gate-1 becomes 0. This forces the $\bar{Q}$ output to 1. Therefore both the inputs to gate-2 is 1. This forces $Q=0$. This is called reset condition.

Case-IV, $S=R=1$

If $S=R=1$ Then, output of gates 1 and gate-2 becomes zero. Hence one of the inputs to gate-2 and 1 will be 0. The output of both the gates Q and $\bar{Q}$ becomes 1. It is not allowed as Q and $\bar{Q}$ should be complementary. So, this state is prohibited.

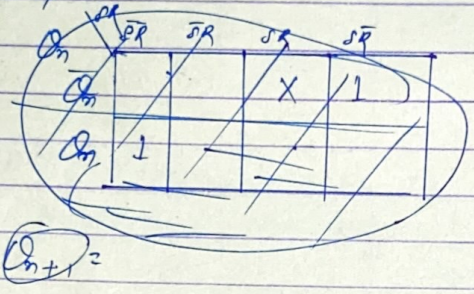
Inputs		outputs				Comment
S	R	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	0	1	0	1	N/C
0	0	1	0	1	0	
0	1	0	1	0	1	RESET
0	1	1	0	0	1	
1	0	0	1	1	0	SET
1	0	1	0	1	0	
1	1	0	1	x	x	PROHIBITED STATE
1	1	1	0	x	x	

Truth Table of S-R latch.

Race condition: when S=1, R=1 then, output Q=1 and $\bar{Q}$=1 this is known as race condition.

Characteristics equation:

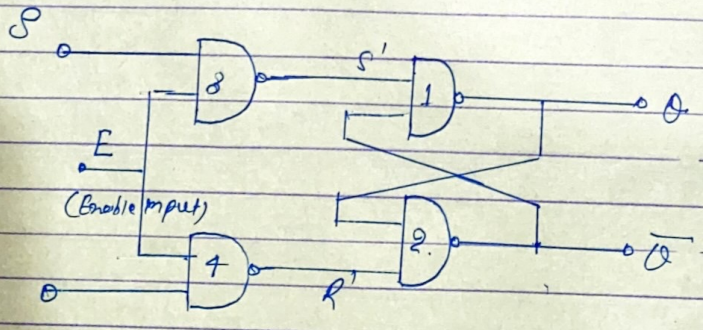
The characteristic equation of a flip-flop is the equation which relates the next state of the flip-flop as later to the current state and inputs.



~~NAND LATCH (SR LATCH USING NAND)~~

THE GATED S-R LATCH (Pve Level Triggered S-R FF)

The figure shows the gated SR latch using NAND gate with an additional enable input. This is known as level triggered SR FF.



Gated SR Latch.

This circuit is enabled only when a E=1. If E=0, then there is no change in the output.

working operations:

Case-I $S = X, R = X, E = 0$

In this case o/p of gate 3 and 4 is 1 irrespective of the value of S and R; there is no change of output Q and $\bar{Q}$.

Case-II : $S = R = 0$. No change.

Under this case, o/p of both of gate 3 and 4 are forced to become 1 and hence S' and R' are equal to 1. So, There is no change in o/p.

Case-III $S = 0, R = 1$ Rest condition.

$E = 1$

Under this case output of G-3 is 1 i.e $S' = 1$ and output of G-4 is 0 i.e $R' = 1$

Hence $Q_{n+1} = 0$ and $\bar{Q}_{n+1} = 1$. This is called RESET condition.

Case-IV: $S = 1, R = 0, E = 1$.

Under this case o/p of Gate-3 is 1 i.e $S' = 1$ and o/p of Gate-4 is 0 i.e $R' = 0$.

This is the condition of Set.

Case-V $S = 1, R = 1$ $E = 1$

Under this case output of both gate-3 and gate-4 is 0, then o/p of both gate forced to 1. called race condition.

Case	Inputs: Enable(E)	S	R	outputs: Q_{n+1}	$\bar{Q}_{n+1}$	Comments
I	0	X	X	Q_n	$\bar{Q}_n$	No change in E=0
II	1	0	0	Q_n	$\bar{Q}_n$	NC.
III	1	0	1	$\bar{Q}_n(0)$	Q_{n+1}	RESET
IV:	1	1	0	$Q_n(1)$	$\bar{Q}_{n+1} = 0$	SET
V	1	1	1	Indeterminate		Avoid this condition.